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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/641,035	08/16/2000	David Wallman	SUN1P275/P4783	3756

22434 7590 03/15/2004

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EXAMINER	
KANG, INSUN	
ART UNIT	**PAPER NUMBER**
2124	

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/641,035	WALLMAN, DAVID	
	Examiner	Art Unit	
	Insun Kang	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/16/2000, 8/20/2001 and 2/17/2004.*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed 8/16/2000, 8/20/2001 and 2/17/2004.

2. Claims 1-24 are pending in the application

Specification

3. The disclosure is objected to because of the following informalities: the phrases "frames114" in pg 6 line 22 needs to be changed to "frames 114a-f"; "first instruction 106," in pg 6 line 28, to "first instruction 106a"; "106d," in pg 7 line 2, to "106d"; "250, 252," in pg 9 line 10, to "270, 272"; "bytecode 406...418," in pg 11 lines 32-33, to "bytecodes 406 a-b...418a-b."

The specification uses the sentence "determining when the program instruction is a branch instruction," it needs to be changed either to "determining if the program instruction is a branch instruction" or the verb "determine" needs direct objects to complete its meaning as it is unclear what is to be determined when the program instruction is a branch instruction. The sentence, "determining when a basic block is present in a code cache when it is determined that the program instruction is a branch instruction," needs to be corrected for the same reason set forth above.

Appropriate correction is required.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because the abstract uses phrases that can be implied such as "Methods ...are disclosed," in the first sentence and "According to one aspect of the present invention," in line 2 and "In one embodiment," in line 11. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-18 and 22-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claim 1, the sentence, "determining when the program instruction is a branch instruction," is unclear whether it was meant to be "determining if the program instruction is a branch instruction" or what is to be determined when the program instruction is a branch instruction is simply missing by mistake. It is interpreted as

"determining if the program instruction is a branch instruction." The sentence, "determining when a basic block is present in a code cache when it is determined that the program instruction is a branch instruction," is interpreted as "determining if a basic block is present in a code cache if it is determined that the program instruction is a branch instruction," and the sentence, "executing the code included in the basic block when it is determined that the basic block is present," as "executing the code included in the basic block if it is determined that the basic block is present," for the same reasons set forth above.

Per claims 5, 9-12 and 16-18, these claims are rejected for the same reasons set forth in claim 1.

Per claims 2-4, 6-8, 13-15, these claims are rejected for dependency on the above rejected parent claim 1 and 11.

The term "substantially" in claims 5 and 22 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Regarding claims 23 and 24, these claims are rejected for dependency on the above rejected parent claim 22.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Walters et al. (U.S. Patent 5,768,593).

Per claim 22:

Walters teaches:

-a processor (see Fig 1)

-an interpreter("instruction is executed by the interpreter," col 4 lines 1-2)

-a native code cache, the native code cache being associated with the processor ("the native code block in the code cache," col 3 lines 55-60; Fig 2-5)

-wherein the interpreter includes at least one block of binary code that is arranged to be copied substantially directly into the native code cache("After the native code is generated, the resulting native code block is stored in the code cache, an entry for the stored code block is generated in the hash table," col 13 lines 5-30; Fig 2-5).

Per claim 23:

The rejection of claim 22 is incorporated, and further, Walters teaches that the at least one block of binary code is associated with a bytecode which is arranged to be interpreted by the interpreter("it is determined that the entry point instruction is one of a predefined set of non-native instructions to be executed by an interpreter, then that instruction is executed by the interpreter," col 3 lines 65-67; col 4 lines 1-3).

Per claim 24:

The rejection of claim 23 is incorporated, and further, Walters teaches that the at least one block is arranged to include indirect calls (col3 lines 35-65; Fig 2-5).

Per claim 1:

Walters discloses:

-obtaining a program instruction to be executed by the virtual machine ("instruction is executed by the interpreter," col 4 lines 1-4)

-determining when the program instruction is a branch instruction ("a branch instruction flag that is set true only for qualifying instructions that are branch instructions," col 10 lines 11-36; col 5 lines 10-40)

-determining when a basic block is present in a code cache when it is determined that the program instruction is a branch instruction, the basic block including code, the code cache being associated with the virtual machine ("the hash table to see if a corresponding native code block is already stored in the code cache," col 3 lines 34-64; Fig 2-5)

-executing the code included in the basic block when it is determined that the basic block is present ("If so, the native code block in the code cache is executed until an exit instruction in the native code block is encountered," col 3 lines 54-67; Fig 2-5)

Per claim 2:

The rejection of claim 1 is incorporated, and further, Walters teaches:

-when it is deterimned that the basic block is not present in the code cache, the method further

("if there is no corresponding native code block is in the code cache," col 3 lines 60-67)

-interpreting the program instruction (col 3 lines 60-67; col 4 lines 1-3; Fig 2-5)

-copying code corresponding to the program instruction into the code cache ("After the native code is generated, the resulting native code block is stored in the code cache, an entry for the stored code block is generated in the hash table," col 13 lines 5-30; Fig 2-5)

Per claim 3:

The rejection of claim 2 is incorporated, and further, Walters teaches:

-allocating space in the code cache for the code corresponding to the program instruction ("After the native code is generated, the resulting native code block is stored in the code cache, an entry for the stored code block is generated in the hash table," col 13 lines 5-30; Fig 2-5)

-providing the code corresponding to the program instruction with a label (col 10 lines 29-47; Fig 2-5).

Per claim 4:

The rejection of claim 3 is incorporated, and further, Walters teaches placing the label in a table of labels (col 7 lines 24-36; Fig 2-5)

Per claim 5:

The rejection of claim 2 is incorporated, and further, Walters teaches:

-searching through a table of labels to determine if a target associated with the program Instruction has a substantially matching label in the table of labels ("hash table lookup procedure to look up the address of the entry point instruction in the hash table to see if a corresponding native code block is already stored in the code cache," col 7 lines 15-24; "The use of the code chunk map enables...to efficiently identify all code blocks in the code cache," col 8 lines 46-63; Fig 2-5)

Per claim 6:

The rejection of claim 2 is incorporated, and further, Walters teaches:

the program instruction is a bytecode, and wherein the bytecode is executed by an interpreter of the virtual machine ("it is determined that the entry point instruction is one of a predefined set of non-native instructions to be executed by an interpreter, then that instruction is executed by the interpreter," col 3 lines 65-67; col 4 lines 1-3).

Per claim 7:

The rejection of claim 2 is incorporated, and further, Walters teaches:

the code cache is a native code cache, and the code corresponding to the program instruction is native code("the native code block in the code cache is executed until an exit instruction in the native code block is encountered," col 3 lines 54-67)

Per claim 8:

The rejection of claim 1 is incorporated, and further, Walters teaches:

the program instruction is a bytecode ("non-native code,"col 3 lines 35-44) and the code cache is a native code cache ("native code block in the code cache," col 3 lines 55-60)

Per claim 9:

The rejection of claim 1 is incorporated, and further, Walters teaches:

-interpreting the bytecode when it is determined that the program instruction is not the branch instruction(col 3 lines 60-67; col 4 lines 1-3)

Per claim 10:

The rejection of claim 1 is incorporated, and further, Walters teaches:

-computing a target using the program instruction, wherein determining when the basic block is present in the code cache includes determining if the code cache includes any basic blocks which correspond to the target (col 5 lines 10-40; col 7 lines 24-63; Fig 2-5).

Per claims 11-14, these are the computer program product versions of claims 1-4 and 8, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 1-4 and 8 above.

Per claim 15:

The rejection of claim 11 is incorporated, and further, Walters teaches that the computer-readable medium is one selected from the group consisting of a data signal embodied in a carrier wave, a floppy disk, a computer memory, a hard disk, an optical disk, a tape drive, and a CD-ROM. Bytecodes can be executed on any computer system with a virtual machine, therefore, accordingly, Walters anticipates this claim.

Per claim 16:

Walters discloses:

-a code cache ("a hash table for lactating code blocks in the code cache," col 3 lines 35-44)

-an interpreter, the interpreter being arranged to obtaining a bytecode ("instruction is executed by the interpreter," col 4 lines 1-4)

-the interpreter further being arranged to determining when the bytecode is a branch bytecode ("a branch instruction flag that is set true only for qualifying instructions that are branch instructions," col 10 lines 11-36; col 5 lines 10-40)

-to determine when a basic block is present in the code cache when it is determined that the bytecode is a branch bytecode, the basic block including native code ("the hash table to see if a corresponding native code block is already stored in the code cache," col 3 lines 34-64; Fig 2-5)

-wherein the interpreter causes the native code to be executed when it is determined that the basic block is present("If so, the native code block in the code cache is executed until an exit instruction in the native code block is encountered," col 3 lines 54-67; Fig 2-5)

Per claim 17:

The rejection of claim 16 is incorporated, and further, Walters teaches that the interpreter is further arranged to interpret the bytecode (col 3 lines 60-67; col 4 lines 1-3) when it is determined that the basic block is not present in the code cache ("if there is no corresponding native code block is in the code cache," col 3 lines 60-67) and to copy

native code corresponding to the bytecode into the code cache("After the native code is generated, the resulting native code block is stored in the code cache, an entry for the stored code block is generated in the hash table," col 13 lines 5-30)

Per claim 18:

The rejection of claim 16 is incorporated, and further, Walters teaches that the interpreter is further arranged to interpret the bytccode (col 3 lines 60-67; col 4 lines 1-3)when it is determined that the bytecode is not a branch bytecode ("if there is no corresponding native code block is in the code cache," col 3 lines 60-67).

Per claim 19:

Walters discloses

-identifying a portion of compiled code which corresponds to a block of source code("the hash table to see if a corresponding native code block is already stored in the code cache," col 3 lines 34-64; Fig 2-5)

-copying the portion of compiled code into a code cache("After the native code is generated, the resulting native code block is stored in the code cache, an entry for the stored code block is generated in the hash table," col 13 lines 5-30; Fig 2-5).

Per claim 20:

The rejection of claim 19 is incorporated, and further, Walters teaches that the code cache is a native code cache, and the portion of compiled code is native code("the

native code block in the code cache is executed until an exit instruction in the native code block is encountered," col 3 lines 54-67; Fig 2-5)

Per claim 21:

The rejection of claim 20 is incorporated, and further, Walters teaches executing the portion of compiled code copied into the native code cache using a processor("it is determined that the entry point instruction is one of a predefined set of non-native instructions to be executed by an interpreter, then that instruction is executed by the interpreter," col 3 lines 65-67; col 4 lines 1-3; Fig 2-5).

10. Claims 1, 11, 16, 19 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Adams(U.S. Patent 5,889,996).

Per claim 1:

Adams discloses:

-obtaining a program instruction to be executed by the virtual machine (col 4 lines 53-60)

-determining when the program instruction is a branch instruction(col 15 lines 45-67; col 16 lines 1-9);

-determining when a basic block is present in a code cache when it is determined that the program instruction is a branch instruction, the basic block including code, the code cache being associated with the virtual machine (col 15 lines 45-64; col 12 lines 6-17 and 60-67)

-executing the code included in the basic block when it is determined that the basic block is present (col 12 lines 6-17).

Per claim 11, this is the computer program product version of claim 1, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 1 above.

Per claim 16:

Adams discloses:

-a code cache ("code cache," abstract)

-an interpreter (abstract)

-the interpreter being arranged to obtaining a bytecode, the interpreter further being arranged to determining when the bytecode is a branch bytecode(col 15 lines 45-67; col 16 lines 1-9) and to determine when a basic block is present in the code cache when it is determined that the bytecode is a branch bytecode, the basic block including native code, col 15 lines 45-64; col 12 lines 6-17 and 60-67)

wherein the interpreter causes the native code to be executed when it is determined that the basic block is present(col 12 lines 6-17).

Per claim 19:

Adams discloses:

-identifying a portion of compiled code which corresponds to a block of source code (col 12 lines 6-25 and 52-67)

-copying the portion of compiled code into a code cache (col 11 lines 33-41; col 12 lines 52-67).

Per claim 22:

Adams discloses:

-a processor (Fig 4);

-an interpreter(abstract)

-a native code cache, the native code cache being associated with the processor(col 11 lines 33-51),

-wherein the interpreter includes at least one block of binary code that is arranged to be copied substantially directly into the native code cache (col 11 lines 52-56).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Insun Kang whose telephone number is 703-305-6465. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on 703-305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IK
3/5/2004

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